ABSTRACT

A memory cell includes: a charge storage element (e.g., capacitor); a switch constructed and arranged to selectively connect the charge storage element to a first data line, responsive to a first select signal; and a gain element having an input connected to receive a signal from the capacitor and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal. The switch can be a FET having a drain connected to the first data line, a source connected to the capacitor and a gate connected to the first select signal. The gain element can be a FET having a gate connected to the capacitor, a source connected to the second data line and a drain selectively connected to one of an upper power supply and a lower power supply. The switch can transfer a signal from the first data line onto the capacitor and can transfer a signal from the capacitor onto the first data line when selected by the first select signal. A two-dimensional array of such memory cells can be formed, wherein the first select signal and the second select signal orthogonally select cells, to facilitate matrix pivot operations and bit interleave/de-interleave operations. Also, a method of addressing an array of such memory cells can comprise: writing groups of bits linearly arrayed with respect to each other; and reading groups of bits linearly arrayed with respect to each other and orthogonally disposed to the groups of bits written.